

Appl. No. 09/531,135  
Amdt. Dated July 11, 2005  
Reply to Office Action of April 20, 2005

Attorney Docket No. 81784.0027  
Customer No.: 26021

**Amendments to the Drawings:**

The attached sheet of drawing includes a change to Fig. 3. This sheet, which includes Figs. 3 and 4, replaces the original sheet including Figs. 3 and 4. In Fig. 3, the subtraction result "D1" has been changed to "D1'" as suggested in the Office Action.

Attachment: Replacement Sheet

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**REMARKS/ARGUMENTS**

Claims 1-11 are pending in the application. By this amendment, claims 1, 7 and 11 are being amended to improve their form. No new matter is involved.

In paragraph 3 which begins on page 2 of the Office Action, the drawings are objected to because the subtraction result "D1" in Fig. 3 should read "D1'", as described at line 4 of page 12. In response, Applicant is enclosing a replacement sheet which includes Figs. 3 and 4 and which replaces the original sheet including Figs. 3 and 4. In Fig. 3 of the replacement sheet, the subtraction result "D1" has been corrected to read "D1'". Accordingly, the objections to the drawing have now been overcome.

Claims 2-6 and 8-10 are allowed in the Office Action.

In paragraph 5 on page 3 of the Office Action, claims 1, 7 and 11 are rejected Under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent 6,002,425 of Yamanaka et al. In response, Applicant is amending claims 1, 7 and 11 in order to clearly distinguish patentably over Yamanaka.

Applicant has reviewed the Yamanaka et al. reference. While such reference discloses a structure in which signals supplied from pixels at odd and even rows of the CCD are stored in different memories and signal data of pixels at odd and even rows are added together in a connector circuit, the reference does not describe a means corresponding to the "timing control circuit" of the present invention "for setting a storage time of information charges at the first light receiving pixel and a storage time of information charges at the second light receiving pixel". In other

words, Yamanaka does not describe a means for separately setting information charge setting time periods relative to pixels at odd and even rows, respectfully.

According to the present invention, because an information charge setting time can be separately set for the first and second light receiving pixels, it is possible to set different values of light amounts for the first and second light receiving pixels, at which the storage level of information charge saturates. This enables expansion of the dynamic range of the solid state-image pickup apparatus. Yamanaka cannot achieve this advantage because it lacks a means for separately setting information charge setting periods relative to pixels at odd and even rows, respectively.

U.S. Patent 6,441,851 of Yonemoto is cited in the Office Action but is not applied in rejecting the claims. However, Yonemoto is said to disclose a solid-state image pickup device including alternating columns of first and second light receiving pixels wherein the first and second light receiving pixels have mutually different accumulation times and are added together, so that such reference is considered pertinent to Applicant's disclosure.

Applicant has reviewed the Yonemoto reference. Such reference describes a structure in which information charges are stored in pixels at odd and even rows for a long period of time and then are added together to produce a long accumulation time signal, and thereafter, information charges are again stored in pixels at odd and even rows for a short period of time and then added together to produce a short accumulation time signal.

It can be assumed that this "long or short accumulation time signal" in Yonemoto corresponds to the information charge resulting from addition of the

information charges stored in the first and second light receiving pixels in the present invention. Because it can also be assumed that pixels at odd and even pixels (or even and odd pixel) in Yonemoto respectively correspond to the first and second light receiving pixels, it appears that Yonemoto discloses a structure corresponding to the structure of the present invention, in which information charges stored in the first and second light receiving pixels are added.

However, inasmuch as Yonemoto does not describe a structure in which information charge stored in a pixel at an odd (or even) row is added to a long (or short) accumulation time signal, such reference does not describe a structure in accordance with the present invention in which information charge stored in the first light receiving pixel is added to the information charge resulting from addition of the information charges stored in the first and second light receiving pixels.

Claim 1 as amended herein defines a solid-state image pickup apparatus which includes “a solid-state image pickup device”, “a drive circuit for driving the first and second light receiving pixels”, a timing control circuit” and “a signal processing circuit”. As amended herein, claim 1 recites “wherein after driving the first and second light receiving pixels to accumulate information charges in the first and second light receiving pixels, the drive circuit adds information charges accumulated in the first light receiving pixel and information charges accumulated in the second light receiving pixel, and, the drive circuit drives the first and second light receiving pixels to further accumulate information charges in the first and second light receiving pixels and further adds information charges accumulated in the first light receiving pixels and the added information charges”. Claims 7 and 11 as amended herein, contain similar language. Therefore, such claims are submitted

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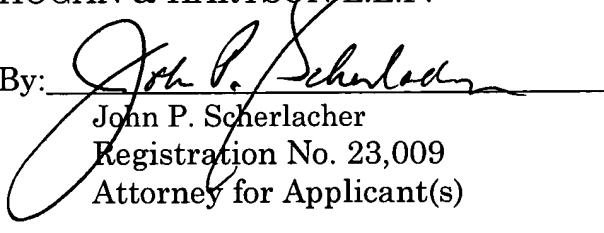
to clearly distinguish patentably over Yamanaka et al. which is applied in rejecting such claims and Yonemoto which is said to be pertinent to Applicant's disclosure.

In conclusion, claims 1, 7 and 11 are submitted to clearly distinguish patentably over the prior art, in addition to claims 2-6 and 8-10 which have been allowed. Therefore, reconsideration and allowance are respectfully requested.

If there are any fees due in connection with the filing of this response, please charge the fees to our Deposit Account No. 50-1314.

Respectfully submitted,  
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